Remarks

Claims 1-20 are pending in this application. Claims 1, 8, and 15 have been amended to clarify the present invention. The examiner has rejected claims 1-20 as anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 6,282,601 to Goodman et al, hereinafter Goodman. The applicant respectfully traverses the examiner's rejections in so far as they may apply to the newly amended claims.

A. Independent Claims 1, 8, and 15

The Examiner has rejected claims 1, 8, and 15 under 35 U.S.C. § 102(b) as being anticipated by Goodman. A rejection under Section 102(b) requires that each element of the rejected claim or claims be disclosed in a single prior art reference. As such, because the examiner rejected claims 1, 8, and 15 under Section 102 on the basis of Goodman, each element of these claims must be disclosed in Goodman. Goodman, however, does not disclose each element of amended independent claims 1, 8, and 15. Specifically, Goodman does not disclose a uniquely addressable semaphore associated with each processor to indicate "whether the associated processor has exited the interrupt mode."

Amended independent claims 1 and 15 recite a system where a uniquely addressable semaphore is associated with each processor and indicates whether the associated processor has exited the interrupt mode. Similarly, amended independent claim 8 recites a method comprising the step of setting a semaphore associated with the processor to indicate whether the processor has exited the interrupt mode. Once an interrupt request such as a SMI has been asserted, all the processors in a multiple processor system will go into interrupt mode, even though only one processor will actually be selected to handle the interrupt. (Specification, page 3, ll. 10-11.) A semaphore is an indicator bit or a "flag" which is set by the processors in order to

manage their entry into and exit from the interrupt mode. (Specification, page 3, ll. 12-15.) The establishment of semaphores for each processor permits each semaphore to be accessed independently of the other semaphores and eradicates the need for an exclusive or atomic access to the semaphores. (Specification, page 5, ll. 8-16.) Therefore, the semaphores disclosed in the present invention indicate *which of the processors in a multi-processor system are in interrupt mode and which ones have exited the interrupt mode.*

On the other hand, Goodman is directed to a data processing system and method for *identification of the processor requesting the interrupt.* (Col. 2, ll. 1-5.) A request for a system management interrupt (SMI) within a multi-processor system causes the state of at least the requesting processor to be saved. (Col. 2, ll. 8-12.) Each processor's saved state includes contents of at least one internal software variable register of the requesting processor which contains an identifying signature. (Col. 2, ll. 12-15.) Once the SMI handler is executed, it will use the contents of the internal software variable register to identify the requesting processor. (Col. 2, ll. 15-20.) Thus, Goodman addresses a method and system for identifying the requesting processor when handling an interrupt. In contrast, the present application discloses a method and system that comes into play after the processors have entered the interrupt mode and the interrupt handling process has been initiated, which can identify the processors that remain in interrupt mode, and those which have exited the interrupt mode.

The examiner points to the following section in Goodman as a disclosure of this feature:

> [i]nterrupt hardware 60 responds to an SMI request being written into SMI request register 62 by asserting an SMI interrupt to all of processors 12. Although each of processors 12 accepts the SMI, only the boot processor (e.g., system processor 12*a*) executes an SMI handler to service the SMI, as described in greater detail

> below with respect to FIG. 4. Meanwhile, as shown at block 108, the requesting processor (i.e., system processor 12*b*) suspends execution of its process and stores the state of the process, including the contents of register file 78 and other volatile data of system processor 12*b*, to memory (e.g., system memory 16). Depending upon implementation, some or all of the other system processors 12 will similarly save the states of their processes and suspend execution.

(Goodman, Col. 4, ll. 54-67). The recited paragraph, however, merely discloses the steps involved in identification of the requesting processor and is completely silent as to the use of a semaphore that would indicate whether its associated processor has exited the interrupt mode. Therefore, Goodman fails to disclose a uniquely addressable semaphore which *indicates whether the associated processor has exited the interrupt mode* as disclosed by amended independent claims 1, 8, and 15 of the present application.

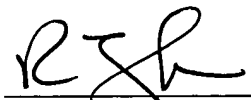
B. The Rejection of Dependent Claims 2-7, 9-14, and 16-20 on Section 102 Grounds

The rejection of dependent claims 2-7, 9-14, and 16-20 on Section 102 grounds will not be discussed individually herein, as each of these claims depends, either directly or indirectly, from an otherwise allowable base claim.

Conclusion

The applicant respectfully submits that the pending claims 1-20 of the present invention, as amended, are allowable. The applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,



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